THE INVENTION CLAIMED IS:

1. A method for manufacturing an electrostatic discharge protection structure comprising the steps of:

providing a semiconductor substrate;

forming a shallow trench opening in the semiconductor substrate

implanting source and drain diffusion regions in the semiconductor substrate;

implanting source and drain wells respectively under the source and drain diffusion regions in the semiconductor substrate;

forming a shallow trench isolation over the semiconductor substrate and in the shallow trench opening in the semiconductor substrate to separate the source and drain diffusion regions and a portion of the source and drain wells; and

forming source and drain contact structures on the shallow trench isolation respectively over the source and drain diffusion regions and through the shallow trench isolation to contact the source and drain diffusion regions.

2. The method for manufacturing an electrostatic discharge protection structure as claimed in claim 1 wherein the step of:

implanting the source and drain wells implants source and drain wells of a first conductivity type; and

including a step of:

implanting a source and a drain implant of a second conductivity type individually bridging the source and drain wells at the bottoms thereof to the semiconductor substrate.

3. The method for manufacturing an electrostatic discharge protection structure as claimed in claim 1 wherein the steps of:

forming the shallow trench isolation forms source and drain openings therein; and

forming the source and drain contact structures forms the respective source and drain contact structures extending through the source and drain openings to respectively contact the source and drain diffusion regions.

4. The method for manufacturing an electrostatic discharge protection structure as claimed in claim 1 wherein the step of:

forming the source and the drain wells forms the source and drain wells spaced proximate each other whereby the minimum value for efficient bipolar turn-on time is achieved.

5. A method for manufacturing an electrostatic discharge protection transistor comprising the steps of:

providing a semiconductor p-substrate;

forming a shallow trench opening in the semiconductor p-substrate;

implanting n+ source and n+ drain diffusion regions in the semiconductor p-substrate on both sides of the shallow trench opening;

implanting respective source and drain n-wells under the n+ source and n+ drain diffusion regions in the semiconductor p-substrate;

forming a shallow trench isolation over the semiconductor p-substrate and into the semiconductor p-substrate to separate the n+ source and n+ drain diffusion regions and portions of the source and drain n-wells; and

forming source and drain contact structures respectively formed on the shallow trench isolation over the n+ source and n+ drain diffusion regions and extending through the shallow trench isolation to contact the n+ source and n+ drain diffusion regions;

6. The method for manufacturing an electrostatic discharge protection transistor as claimed in claim 5 including:

forming source and drain openings in the shallow trench isolation respectively open to the n+ source and n+ drain diffusion regions; and

implanting a p- source and a p- drain implant respectively through the source and drain openings to individually bridge the source and drain n-wells to the semiconductor p-substrate.

7. The method for manufacturing an electrostatic discharge protection transistor as claimed in claim 5 wherein the steps of:

implanting the n+ source and n+ drain diffusion regions form regions having proximate and distal edges;

forming the shallow trench isolation forms source and drain contact openings therein between the proximate and distal edges of the n+ source and n+ drain diffusion regions and open thereto; and

forming the source and drain contact structures form the source and drain contact structures respectively in through the source and drain contact openings to contact the n+ source and n+ drain diffusion regions.

8. The method for manufacturing an electrostatic discharge protection transistor as claimed in claim 5 wherein the step of:

implanting the source and the drain n-wells implants the source and drain n-wells spaced apart by the shallow trench isolation a portion of the depths thereof from a surface of the semiconductor p-substrate but proximate each other whereby the minimum value for efficient bipolar turn-on time is achieved and the snapback breakdown occurs distally from the surface of the semiconductor p-substrate.

9. An electrostatic discharge protection structure comprising:

a semiconductor substrate, the semiconductor substrate having source and drain diffusion regions, the semiconductor substrate having respective source and drain wells under the source and drain diffusion regions;

a shallow trench isolation formed over the semiconductor substrate and into the semiconductor substrate to separate the source and drain diffusion regions and a portion of the source and drain wells; and

source and drain contact structures respectively formed on the shallow trench isolation over the source and drain diffusion regions and extending through the shallow trench isolation to contact the source and drain diffusion regions.

10. The electrostatic discharge protection structure as claimed in claim 9 wherein:

the source and drain wells are of a first conductivity type; and

including:

a source and a drain implant of a second conductivity type individually bridging the source and drain wells to the semiconductor substrate.

11. The electrostatic discharge protection structure as claimed in claim 9 including:

a gate located between the source and drain contact structures.

12. The electrostatic discharge protection structure as claimed in claim 9 wherein:

the source and the drain wells are spaced proximate each other whereby the minimum value for efficient bipolar turn-on time is achieved.

13. An electrostatic discharge protection transistor comprising:

a semiconductor p-substrate, the semiconductor p-substrate having n+ source and n+ drain diffusion regions, the semiconductor p-substrate having respective source and drain n-wells under the n+ source and n+ drain diffusion regions;

a shallow trench isolation formed over the semiconductor p-substrate and into the semiconductor p-substrate to separate the n+ source and n+ drain diffusion regions and portions of the source and drain n-wells; and

source and drain contact structures respectively formed on the shallow trench isolation over the n+ source and n+ drain diffusion regions and extending through the shallow trench isolation to contact the n+ source and n+ drain diffusion regions;

14. The electrostatic discharge protection transistor as claimed in claim 13 including:

a p- source and a p- drain implant individually bridging the source and drain n-wells to the semiconductor p-substrate.

15. The electrostatic discharge protection transistor as claimed in claim 13 wherein:

the n+ source and n+ drain diffusion regions have proximate and distal edges;

the shallow trench isolation has source and drain contact openings provided therein between the proximate and distal edges of the n+ source and n+ drain diffusion regions and open thereto; and

the source and drain contact structures respectively extend through the source and drain contact openings to respectively contact the n+ source and n+ drain diffusion regions.

16. The electrostatic discharge protection transistor as claimed in claim 13 wherein:

the source and the drain n-wells are spaced apart by the shallow trench isolation a portion of the depths thereof from a surface of the semiconductor p-substrate but proximate each other whereby the minimum value for efficient bipolar turn-on time is achieved and the snapback breakdown occurs distally from the surface of the semiconductor p-substrate.